Multi-function Input/Output Driver

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FIELD OF INVENTION

[0001] The present invention relates generally to integrated circuits and specifically to input/output (I/O) drivers for integrated circuits.

DESCRIPTION OF RELATED ART

[0002] Changing system requirements are driving the need for high bandwidth input/output (I/O) interface standards support. Thus, higher performance systems, driven by faster processors and memories, are increasing the need for higher bandwidth data transfers. In response to these system changes, new I/O standards are continually emerging. For example, many modern processing systems use the High Speed Transceiver Logic (HSTL) standard for data transfers to and from memory, and use the Low Voltage Differential Signaling (LVDS) standard for backplane communications.

[0003] The HSTL standard, which includes several classes, specifies the output characteristics for single-ended outputs having both series terminating loads (Class II) and parallel terminating loads (Classes (I, III, and IV). The HSTL standard does not specify device supply voltages, thereby making it a process-independent standard. For example, the HSTL Class I standard specifies an input reference voltage $V_{REF} = V_{DD}/2$ and an output terminated to $V_{TT} = V_{DD}/2$, where V_{DD} is the supply voltage. FIG. 1 illustrates a typical HSTL Class I output driver 100. Driver 100 includes a CMOS inverter formed by a PMOS transistor 102 and an NMOS transistor 104 connected in series between V_{DD} and ground potential. An input signal IN is provided to the

gates of transistors 102 and 104, and a complementary output signal OUT is generated in response thereto. The output is terminated to V_{TT} via a 50 ohm load resistor R_L.

[0004] The LVDS standard is a differential signaling standard that specifies a common mode voltage of 1.2 volts and a logic swing of approximately 345 milli-volts between the logic high and logic low levels. Typically, a 100 ohm termination resistor is coupled between the differential signal lines. For example, FIG. 2 illustrates a typical LVDS driver 200. Driver 200 includes a differentially coupled pair of NMOS transistors 202 and 204 biased with a current source 210. The gates of transistors 202 and 204 receive a differential signal defined by input signals IN1 and IN2. PMOS load transistors 206 and 208, which are coupled between the differential pair 202/204 and V_{DD}, each receive a bias control voltage Vbias. The differential voltage between IN1 and IN2 causes transistors 202 and 204 to steer current either through load transistor 206 or load transistor 208 to generate a differential signal between OUT1 and OUT2.

[0005] Typically, I/O drivers provide functionality for a specific type of signaling, i.e., either single-ended or differential, and therefore offer little flexibility in handling signals specified by varying standards. As a result, applications that utilize signals specified by different I/O standards typically require different types of I/O drivers, which in turn increases circuit complexity and silicon area. Thus, there is a need for an I/O driver having common circuitry that can be configured to process signals specified by different I/O standards such as, for example, the HSTL and LVDS signal standards.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The features and advantages of the present invention are illustrated by way of example and are by no means intended to limit the scope of the present invention to the particular embodiments shown, and in which:

[0007] FIG. 1 is a circuit diagram of a well-known driver to process single-ended signals;

[0008] FIG. 2 is a circuit diagram of a well-known driver to process differential signals;

[0009] FIG. 3 is a simplified block diagram of a multi-function driver in accordance with the present invention;

[0010] FIG. 4 is a simplified circuit diagram illustrating an exemplary single-ended configuration for the driver of FIG. 3;

[0011] FIG. 5 is a simplified circuit diagram illustrating an exemplary differential configuration for the driver of FIG. 3;

[0012] FIG. 6 is a circuit diagram of one embodiment of the pull-up circuit of FIG. 3;

[0013] FIG. 7 is a circuit diagram of one embodiment of the pull-down circuit of FIG. 3;

[0014] FIG. 8 is a simplified circuit diagram for one embodiment of the switch matrix of FIG. 3;

[0015] FIG. 9A is circuit diagram for one embodiment of a bias circuit for drivers of the present invention;

[0016] FIG. 9B is a simplified circuit diagram modeling the bias circuit of FIG. 9A;

[0017] FIG. 10 is a block diagram of an interface system employing 16 drivers of FIG. 3; and

[0018] FIG. 11 is a block diagram illustrating an FPGA system employing any number of the drivers of FIG. 3.

[0019] Like reference numerals refer to corresponding parts throughout the drawing figures.

DETAILED DESCRIPTION

[0020] In accordance with the present invention, a high-speed I/O driver is disclosed that can process signals specified by both single-ended and differential I/O standards. The high-speed driver includes circuitry that is configurable to meet single-ended and differential I/O signal standards without the need for different drivers on each I/O pad to implement the various standards, thereby increasing flexibility while minimizing circuit complexity and silicon area.

[0021] In the following description, exemplary embodiments are described in order to provide a thorough understanding of the present invention. For purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details may not be required to practice the present invention. In other instances, well-known circuits and devices are shown in block diagram form to avoid obscuring the present invention unnecessarily. Additionally, the interconnection between circuit elements or blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be a single signal line, and each of the single signal lines may alternatively be a bus. Further, the logic states of various signals described herein are exemplary and therefore may be reversed or otherwise modified as generally known in the art. Accordingly, the present invention is not to be construed as limited to specific examples described herein but rather includes within its scope all embodiments defined by the appended claims.

[0022] FIG. 3 is a simplified block diagram of a multi-function I/O driver 300 configurable to process either single-ended or differential input signals. Driver 300 includes a switch matrix 310, two pull-up circuits 320(1) and 320(2), two

pull-down circuits 330(1) and 330(2), a common mode voltage circuit 340, and switches 350 and 360. Switch matrix 310 includes inputs coupled to I/O pads A and B, outputs coupled to internal signal lines 201-204, and a control terminal to receive a mode signal MODE. Switch matrix 310, which is well-known, selectively routes input signals provided on I/O pads A and B to circuits 320(1), 320(2), 330(1) and 330(2) via signal lines 201-204, respectively. The signal MODE indicates whether input signals provided on I/O pads A and B are to be processed as single-ended signals or as differential signals. For one embodiment, a logic low MODE signal configures driver 300 to process signals as single-ended signals such as, for example, those specified by the HSTL I/O standard, and a logic high MODE signal configures driver 300 to process signals as differential signals such as, for example, those specified by the LVDS I/O standard.

[0023] Pull-up circuit 320(1) is modeled by PMOS transistors MP1 and MP2 connected in series between a supply voltage V_{DD} and a first output node OUT1. The gate of MP1 is coupled to a first bias voltage Vbias_p, and the gate of MP2 is coupled to signal line 201. Pull-up circuit 320(2) is modeled by PMOS transistors MP3 and MP4 connected in series between V_{DD} and a second output node OUT2. The gate of MP3 is coupled to Vbias_p, and the gate of MP4 is coupled to signal line 202. Pull-down circuit 330(1) is modeled by NMOS transistors MN1 and MN2 connected in series between OUT1 and ground potential. The gate of MN1 is coupled to a second bias voltage Vbias_n, and the gate of MN2 is coupled to signal line 203. Pull-down circuit 330(2) is modeled by NMOS transistors MN3 and MN4 connected in series between OUT2 and ground potential. The gate of MN3 is coupled to Vbias_n, and the gate of MN4 is coupled to signal line 204. For other embodiments, other circuit configurations can be used to

implement the pull-up circuits 320 and the pull-down circuits 330.

[0024] Switch 350 has a first terminal connected to a node 321 between PMOS transistors MP1 and MP2 of pull-up circuit 320(1), a second terminal connected to a node 322 between PMOS transistors MP3 and MP4 of pull-up circuit 320(2), and a control terminal to receive MODE. Switch 360 has a first terminal connected to a node 331 between NMOS transistors MN1 and MN2 of pull-down circuit 330(1), a second terminal connected to a node 332 between NMOS transistors MN3 and MN4 of pull-down circuit 330(2), and a control terminal to receive MODE.

[0025] Common mode voltage circuit 340 includes a resistor R1, switches 341-342, and a resistor R2 connected in series between OUT1 and OUT2. For some embodiments, resistors R1 and R2 have a resistance of approximately 100 ohms, although other resistances can be used. Switches 341 and 342 selectively couple corresponding resistors R1 and R2 to a common mode voltage V_{CM} in response to MODE. The common mode voltage, which for some embodiments is 1.2 volts as specified by the LVDS I/O standard, is provided by a well-known voltage supply (not shown for simplicity). For other embodiments, V_{CM} may be a different value, for example, as specified by another differential I/O standard.

[0026] Switches 341, 342, 350, and 360 can be any suitable switch or switching circuit. For some embodiments, switches 341, 342, 350, and 360 are CMOS switches. For one embodiment, switches 341, 342, and 360 are NMOS transistors having gates responsive to MODE, and switch 350 is a PMOS transistor having a gate responsive to $\overline{\text{MODE}}$.

[0027] Output signals OUT1 and OUT2 are generated in response to input signals provided by switch matrix 310 on signal lines 201-204. Output node OUT1 is coupled to I/O pad C via a buffer 370, and output node OUT2 is coupled to I/O pad D via a buffer

380. Buffers 370 and 380 can be any well-known buffers. For other embodiments, buffers 370 and 380 can be eliminated.

[0028] In accordance with the present invention, driver 300 can be configured to process either single-ended signals or differential signals in response to the logic state of MODE. For some embodiments, MODE is a control signal provided by a user. For other embodiments, MODE can be generated by another circuit connected to driver 300. For simplicity, operation of driver 300 for processing single-ended signals is described below with respect to the HSTL I/O standard, and operation of driver 300 for processing differential signals is described below with respect to the LVDS I/O standard. However, embodiments of the present invention can be used to process other single-ended signals (e.g., as specified by GTL, SSTL, TTL, or other I/O standards) and/or to process other differential signals (e.g., as specified by LVPECL or other differential I/O standards).

[0029] To process single-ended (e.g., HSTL) signals, MODE is set to logic low, and two HSTL input signals are provided as IN1 and IN2 to input pads A and B, respectively. In response to the logic low state of MODE, switch matrix 310 routes IN1 from pad A to pull-up circuit 320(1) via line 201 and to pull-down circuit 330(1) via line 203, and routes IN2 from pad B to pull-up circuit 320(2) via line 202 and to pull-down circuit 330(2) via line 204. The logic low state of MODE opens switch 350 to de-couple pull-up circuits 320(1) and 320(2) from each other, and opens switch 360 to de-couple pull-down circuits 330(1) and 330(2) from each other. The logic low state of MODE also opens switches 341-342, thereby de-coupling common mode voltage circuit 340 from driver 300. The first bias voltage Vbias_p is set to a minimum value, e.g., ground potential, to fully turn on transistors MP1 and MP3. The second bias voltage Vbias_n is set to a maximum value, e.g., V_{DD}, to fully turn on transistors MN1

and MN3. The resulting single-ended configuration for driver 300 is represented by an equivalent circuit 400 shown in FIG. 4.

[0030] Thus, referring to FIGS. 3 and 4, when MODE is logic low, pull-up circuit 320(1) and pull-down circuit 330(1) implement an inverting buffer to generate a first single-ended output signal OUT1 in response to the single-ended input signal IN1, and pull-up circuit 320(2) and pull-down circuit 330(2) implement an inverting buffer to generate a second single-ended output signal OUT2 in response to the single-ended input signal IN2. Specifically, transistors MP2 and MN2 form a CMOS inverter that logically inverts IN1 to generate OUT1, with transistors MP1 and MN1 providing suitable source resistances. Similarly, transistors MP4 and MN4 form a CMOS inverter that logically inverts IN2 to generate OUT2, with transistors MP3 and MN3 providing suitable source resistances. Thus, when MODE is logic low, driver 300 can simultaneously process 2 independent single-ended signals.

[0031] For some embodiments, transistors MP1, MP3, MN1, and MN3 are each sized to provide a 50 ohm source resistance as specified, for example, by the HSTL I/O standard. For other embodiments, transistors MP1, MP3, MN1, and MN3 can be sized to provide other source resistances, as may be specified by other I/O standards.

[0032] To process differential (e.g., LVDS) signals, MODE is set to logic high, and an input signal IN1 is provided to pad A. In response to the logic high state of MODE, switch matrix 310 complements IN1 to generate $\overline{IN1}$, thereby generating a differential signal between IN1 and $\overline{IN1}$. Switch matrix 310 can logically invert IN1 to generate $\overline{IN1}$ using any suitable inverting circuit such as, for example, a CMOS inverter. Switch matrix 310 routes IN1 from pad A to pull-up circuit 320(1) via

line 201 and to pull-down circuit 330(1) via line 203, and routes $\overline{IN1}$ to pull-up circuit 320(2) via line 202 and to pull-down circuit 330(2) via line 204. The logic high state of MODE closes switch 350 to couple pull-up circuits 320(1) and 320(2) together, and closes switch 360 to couple pull-down circuits 330(1) and 330(2) together. The logic high state of MODE also closes switches 341-342 to couple common mode voltage circuit 340 between nodes OUT1 and OUT2. The first bias voltage Vbias_p is set to a first predetermined value that causes transistors MP1 and MP3 to provide a desired current flow. The second bias voltage Vbias_n is set to a second predetermined value that causes transistors MN1 and MN3 to provide the desired current flow. The resulting differential configuration for driver 300 is represented by an equivalent circuit 500 shown in FIG. 5.

[0033] Thus, referring to FIGS. 3 and 5, when MODE is logic high, pull-up circuits 320(1) and 320(2) implement a first differential circuit, and pull-down circuits 330(1) and 330(2) implement a second differential circuit. The first and second differential circuits operate to generate a differential output signal between OUT1 and OUT2 in response to the differential input signal between IN1 and $\overline{IN1}$. Specifically, transistors MN2 and MN4 form an NMOS differential pair, and transistors MP2 and MP4 form a PMOS differential pair. Transistors MN1 and MN3 implement a current source to bias the NMOS differential pair MN2/MN4, and transistors MP1 and MP3 implement a current source to bias the PMOS differential pair MP2/MP4. For some embodiments, Vbias_p is selected so that transistors MP1 and MP3 provide a bias current of 8 mA, and Vbias_n is selected so that transistors MN1 and MN3 provide a bias current of 8 mA (as specified, for example, by the LVDS I/O standard). For other embodiments, transistor pairs MP1/MP3 and MN1/MN3 can be

configured to provide other bias currents, as may be required by other differential I/O standards.

[0034] In operation, IN1 is provided to the gates of transistors MP2 and MN2, $\overline{IN1}$ is provided to the gates of transistors MP4 and MN4, and V_{CM} is maintained at 1.2 volts. When IN1 exceeds $\overline{IN1}$, current sourced by transistors MP1 and MP3 flows through transistor MP4, resistors R2 and R1, and transistor MN2 to create a differential signal between OUT2 and OUT1. Conversely, when $\overline{IN1}$ exceeds IN1, current sourced by transistors MP1 and MP3 flows through transistor MP2, resistors R1 and R2, and transistor MN4 to create a differential signal between OUT1 and OUT2. In this manner, driver 300 generates a differential output signal that is centered about V_{CM}.

[0035] Thus, as described above, driver 300 can receive a single-ended signal IN1, invert IN1 to generate $\overline{IN1}$, and then process the differential signal between IN1 and $\overline{IN1}$ to create a differential output signal between OUT1 and OUT2. For other embodiments, a differential input signal can be provided to switch matrix 310 as IN1 and $\overline{IN1}$ on pads A and B, and then processed as described above to generate a corresponding differential output signal between OUT1 and OUT2. For such embodiments, switch matrix 310 routes IN1 from pad A to pull-up circuit 320(1) and to pull-down circuit 330(1), and routes $\overline{IN1}$ from pad B to pull-up circuit 320(2) and to pull-down circuit 330(2).

[0036] The ability of driver 300 to process either single-ended signals or differential signals using the same circuitry eliminates the need to have separate drivers to process single-ended and differential signals, thereby reducing circuit complexity and silicon area. Thus, for example, driver 300 can

be configured to implement either of the I/O configurations shown in FIGS. 1 and 2, or any other driver or input circuit to process various single-ended or differential I/O standards developed in the future. In addition, the ability of driver 300 to process either single-ended signals or differential signals using the same circuitry makes driver 300 suitable for use in logic devices that utilize various signaling standards. For example, driver 300 is ideal for use in FPGA devices that use HSTL I/O standards for memory access and LVDS I/O standards for backplane communications.

[0037] Further, because driver 300 can be used to process either single-ended and differential signals, driver 300 can be sold to customers for use in either single-ended or differential signaling applications, thereby allowing the same configurable driver 300 to compete in various markets once served by a multitude of different I/O drivers. As a result, development, processing, and marketing costs associated with providing separate drivers to satisfy different I/O standards can be minimized.

[0038] FIG. 6 shows a pull-up circuit 600 that is one embodiment of pull-up circuits 320 of FIG. 3. Circuit 600 includes two PMOS transistor pairs 601-602 and 603-604 each connected in series between V_{DD} and the output node OUT. The gates of transistors 602 and 604 receive the input signal IN, and the sources of transistors 602 and 604 are coupled together. The gate of transistor 601 receives a bias voltage Vbias_p_diff, and the gate of transistor 603 receives a bias voltage Vbias_p_se. For some embodiments, transistors 601 and 603 can be modeled as transistor MP1 of pull-up circuit 320(1) and as transistor MP3 of pull-up circuit 320(2), and transistors 602 and 604 can be modeled as transistor MP2 of pull-up circuit 320(1) and as transistor MP4 of pull-up circuit 320(2). The bias

voltages Vbias_p_diff and Vbias_p_se are generated by a suitable bias circuit (not shown in FIG. 6).

[0039] When MODE is logic low, which indicates driver 300 is in the single-ended signal processing mode, Vbias_p_diff is set to a maximum voltage (e.g., V_{DD}) to turn off transistor 601, and Vbias_p_se is set to a minimum voltage (e.g., ground potential) to turn on transistor 603. Thus, during the single-ended mode, transistor 603 provides all the current for transistor pair 602/604. For some embodiments, transistor 603 is sized and doped to provide a 50 ohm load resistance between V_{DD} and transistor pair 602/604 when Vbias_p_se is set to the minimum voltage.

[0040] When MODE is logic high, which indicates driver 300 is in the differential signal processing mode, the gates of transistors 601 and 603 are coupled together and to a predetermined bias voltage Vbias_p_lvds (i.e., Vbias_p_diff = Vbias_p_se = Vbias_p_lvds). Thus, transistors 601 and 603 together act as a current source for transistors 602 and 604. Vbias_p_lvds is set to a level that causes transistors 601 and 603 to provide a desired bias current for the differential operation mode. For one embodiment, transistors 601 and 603 provide 8 mA of current when MODE is logic high, as specified by the LVDS I/O standard.

[0041] For some embodiments, transistors 601 and 603 have much greater current-carrying capacities than transistors 602 and 604, respectively. For some embodiments in which pull-up circuit 600 is fabricated using a 0.2 micron processing technology, transistor 601 has an effective channel width of 30x, transistor 603 has an effective channel width of 6x, transistor 602 has an effective channel width of 14x, and transistor 604 has an effective channel width of 2x.

[0042] FIG. 7 is a pull-down circuit 700 that is one embodiment of pull-down circuits 330 of FIG. 3. Circuit 700

includes two NMOS transistor pairs 701-702 and 703-704 each connected in series between OUT and ground potential. The gates of transistors 702 and 704 receive the input signal IN, and the drains of transistors 702 and 704 are coupled together. The gate of transistor 701 receives a bias voltage Vbias_n_diff, and the gate of transistor 703 receives a bias voltage Vbias_n_se. For some embodiments, transistors 701 and 703 can be modeled as transistor MN1 of pull-down circuit 330(1) and as transistor MN3 of pull-down circuit 330(2), and transistors 702 and 704 can be modeled as transistor MN2 of pull-down circuit 330(1) and as transistor MN4 of pull-down circuit 330(2). The bias voltages Vbias_n_diff and Vbias_n_se are generated by a suitable bias circuit (not shown in FIG. 7).

[0043] When MODE is logic low, which indicates driver 300 is in the single-ended signal processing mode, Vbias_n_diff is set to a minimum voltage (e.g., ground potential) to turn off transistor 701 and Vbias_n_se is set to a maximum voltage (e.g., V_{DD}) to turn on transistor 703. Thus, during the single-ended mode, transistor 703 provides all the current for transistor pair 702/704. Transistor 703 is sized and doped to provide a 50 ohm load resistance between transistor pair 702/704 and ground potential when Vbias_n_se is set to the maximum voltage.

[0044] When MODE is logic high, which indicates driver 300 is in the differential signal processing mode, the gates of transistors 701 and 703 are coupled together and to a predetermined bias voltage Vbias_n_lvds (i.e., Vbias_n_diff = Vbias_n_se = Vbias_n-lvds). Thus, transistors 701 and 703 together act as a current source for transistors 702 and 704. Vbias_n_lvds is set to a level that causes transistors 701 and 703 to provide a desired bias current for the differential operation mode. For one embodiment, transistors 701 and 703 conduct 8 mA of current when MODE is logic high, as specified by

the LVDS I/O standard.

[0045] For some embodiments, transistors 701 and 703 have much greater current-carrying capacities than transistors 702 and 704, respectively. For some embodiments in which pull-down circuit 700 is fabricated using a 0.2 micron processing technology, transistor 701 has an effective channel width of 30x, transistor 703 has an effective channel width of 6x, transistor 702 has an effective channel width of 14x, and transistor 704 has an effective channel width of 2x.

[0046] FIG. 8 is a switch matrix 800 that is one embodiment of switch matrix 310 of FIG. 3. Switch matrix 800 includes multiplexers (MUX) 801 and 802, an inverter 803, and a cross-over circuit 804. MUX 801 includes a first input to receive a first HSTL input signal IN_HSTL1, a second input to receive an LVDS input signal IN_LVDS, a control terminal to receive MODE, and an output coupled to cross-over circuit 804. MUX 802 includes a first input to receive a second HSTL input signal IN_HSTL2, a second input to receive a differential signal $\overline{\text{IN\_LVDS}}$ generated from IN_LVDS by inverter 803, a control terminal to receive MODE, and an output coupled to cross-over circuit 804.

[0047] Cross-over circuit 804 is well-known, and is configured to selectively route the input signals to signal lines 201-204 as described above with respect to FIG. 3. For example, when MODE is logic low, cross-over circuit 804 routes IN_HSTL1 to the inputs of pull-up circuit 320(1) and pull-down circuit 330(1), and routes IN_HSTL2 to the inputs of pull-up circuit 320(2) and pull-down circuit 330(2). When MODE is logic high, cross-over circuit 804 routes IN_LVDS to the inputs of pull-up circuit 320(1) and pull-down circit 330(1), and routes $\overline{\text{IN\_LVDS}}$ to the inputs of pull-up circuit 320(2) and pull-down

circuit 330(2).

[0048] FIG. 9A shows a bias circuit 900 that can be used to generate the bias voltages Vbias_p_diff, Vbias_p_se, Vbias_n_diff, and Vbias_n_se utilized in the embodiments of FIGS. 6 and 7. Bias circuit 900 receives a bias current Ibias from a well-known current source and, in response to MODE, generates the bias voltages Vbias_p_diff, Vbias_p_se, Vbias_n_diff, and Vbias_n_se. Thus, for example, when MODE is logic low to indicate the single-ended processing mode, bias circuit 900 couples Vbias_p_diff and Vbias_n_se to maximum values and couples Vbias_p_se and Vbias_n_diff to minimum values. Specifically, when MODE = 0 and $\overline{\text{MODE}}$ = 1, PMOS transistor 921 is conductive and couples Vbias_p_diff to V_{DD}, PMOS transistor 923 is conductive and couples Vbias_p_se to ground potential, NMOS transistor 931 is conductive and couples Vbias_n_diff to ground potential, and NMOS transistor 933 is conductive and couples Vbias_n_se to V_{DD}. The logic low state of MODE also turns off NMOS transistor 932 to isolate Vbias_n_diff from Vbias_n_se, and the logic high state of $\overline{\text{MODE}}$ turns off PMOS transistor 923 to isolate Vbias_p_diff from Vbias_p_se.

[0049] Conversely, when MODE is logic high to indicate the differential processing mode, bias circuit 900 couples Vbias_p_diff and Vbias_p_se to a first predetermined voltage (e.g., Vbias_p_lvds) and couples Vbias_n_diff and Vbias_n_se to a second predetermined voltage (e.g., Vbias_n_lvds). Specifically, when MODE = 1 and $\overline{\text{MODE}}$ = 0, PMOS transistor 922 turns on and couples Vbias_p_diff and Vbias_p_se together, and NMOS transistor 932 turns on and couples Vbias_n_diff and Vbias_n_se together. The logic high state of MODE also turns off PMOS transistor 921 to isolate Vbias_p_diff from V_{DD}, and turns off PMOS transistor 923 to isolate Vbias_p_diff from ground

potential. The logic low state of $\overline{\text{MODE}}$ turns off NMOS transistor 931 to isolate Vbias_n_diff from ground potential, and turns off NMOS transistor 933 to isolate Vbias_n_se from V_{DD}. PMOS transistors 901-907 and NMOS transistors 911-915 set up the first predetermined bias voltage Vbias_p_lvds for Vbias_p_diff and Vbias_p_se, and set up the second bias voltage Vbias_n_lvds for Vbias_n_diff and Vbias_n_se.

[0050] In response to the logic high state of MODE, NMOS transistor 941 turns on and NMOS transistor 931 turn off, and the bias current Ibias is mirrored through PMOS transistors 905-906 and NMOS transistors 913-914. Because the gates of PMOS transistors 601 and 603 of pull-up circuit 600 are coupled to the gates of PMOS transistors 905 and 906, transistors 601 and 603 mirror a current proportional to Ibias (see also FIG. 6). Similarly, because the gates of NMOS transistors 701 and 703 of pull-down circuit 700 are coupled to the gates of NMOS transistor 942, transistors 701 and 703 mirror a current proportional to Ibias (see also FIG. 7). As mentioned above, transistor pairs 601/603 and 701/703 are configured to conduct a current specified by a selected differential I/O standard (e.g., LVDS).

[0051] Bias circuit 900 can be modeled by the bias circuits 950 and 960 shown in FIG. 9B. PMOS transistors 951, 952, and 953 of circuit 950 correspond to PMOS transistors 921, 922, and 923, respectively, of circuit 900, and NMOS transistors 961, 962, and 963 of circuit 960 correspond to NMOS transistors 931, 932, and 933, respectively, of circuit 900. Resistors 954 and 955 of circuit 950 are connected in series between V_{DD} and ground potential, and implement a voltage divider to set up Vbias_p_lvds at node 956 when MODE is logic high. Similarly, resistors 964 and 965 of circuit 960 are connected in series between V_{DD} and ground potential, and implement a voltage divider

to set up Vbias_n_lvds at node 966 when MODE is logic high.

[0052] FIG. 10 shows an interface circuit 1000 including an arrangement 1006 of 16 drivers 300(1)-300(16) connected in parallel. Each driver 300(1)-300(16) is connected to a corresponding pair of I/O pads 1008(1)-1008(32). The I/O pads 1008(1)-1008(32) are also coupled to outputs of a Synchronous Optical Network (SONET) interface 1002 and to outputs of a 10 Gigabit Attachment Unit Interface (XAUI) 1004.

[0053] SONET interface 1002 receives de-serializes a LVDS serial input signal IN_LVDS into 16 signal channels, and then routes each channel to a corresponding driver 300(1)-300(16) via pads 1008. Referring also to FIG. 3, the switch matrix 310 in each driver 300(1)-300(16) creates a differential input signal from IN_LVDS as described above, e.g., by complementing IN_LVDS to generate $\overline{\text{IN\_LVDS}}$. Thereafter, each driver 300(1)-300(16) processes its differential SONET input signal to generate a corresponding SONET differential output signal in the manner described above.

[0054] XAUI interface 1004 receives 4 pairs of HSTL-compliant single-ended input signals, each of which is 8 bits wide, and routes the resulting 32 input signals to corresponding pads 1008(1)-1008(32). Each driver 300(1)-300(16) receives a pair of these HSTL input signals, and processes them to generate a corresponding pair of HSTL single-ended output signals in the manner described above.

[0055] For other embodiments, arrangement 1006 can include any number of drivers 300, and I/O pads 1008 can be coupled to other interfaces configured to process single-ended and/or differential signals specified by other I/O standards.

[0056] As mentioned above, the ability of present embodiment to process both single-ended and differential signals using the

same circuitry makes driver 300 ideal for use in various logic devices. For example, FIG. 11 shows a system 1100 having a plurality of drivers 300(1)-300(n) having first terminals coupled to an FPGA 1102 and having second terminals coupled to a memory system 1104 and to a backplane 1106. For some embodiments of FIG. 11, drivers 300(1)-300(n) provide HSTL signal buffering between FPGA 1102 and memory system 1104 in the manner described above, and provide LVDS signal buffering between FPGA 1102 and backplane 1106 in the manner described above.

[0057] While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.